Digital Moving Average Filter and its Dynamic Behavior

A moving average filter is a digital filter whose main function is to calculate the average value from a signal. There are several manners to do it. Here, it will be presented one of the simplest manner. It consists only of Delay Blocks. The Fig. 1 presents a simplified representation of system containing a Digital Moving Average Filter.

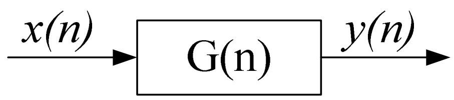

Fig. 1: Simplified representation of a digital moving average filter.

The output *y(n)* is given by (1).

$$y(n)=\frac{1}{N}\sum_{k=n-(N-1)}^{n}x(k) \tag{1}$$

where *N* is the number of samples and *n* is the current sample.

As an example, let's take *N=5*. The equation (1) leads to:

$$y(n)=\frac{1}{5}\sum_{k=n-4}^{n}x(k) \tag{2}$$

which may be written as:

$$y(n)=\frac{1}{5}\left[x(n)+x(n-1)+x(n-2)+x(n-3)+x(n-4)\right] \tag{3}$$

The Fig. 2 presents the block diagram of the digital moving average filter covered in the example.

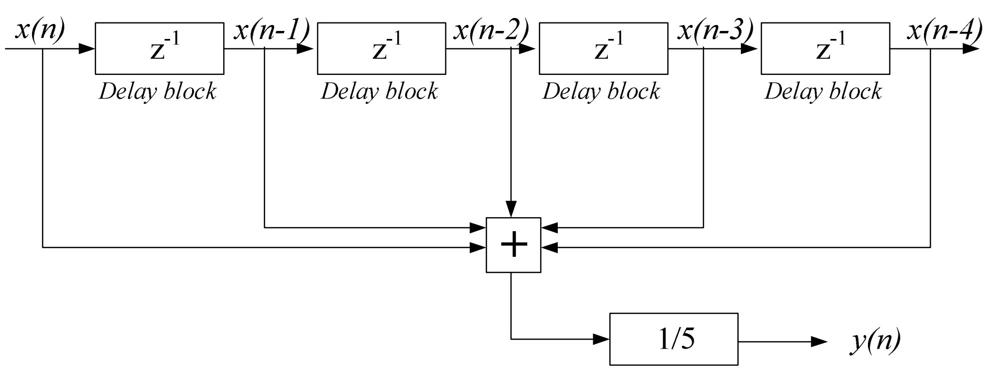

Fig. 2: Block Diagram of the Digital Moving Average Filter.

The value of *N* may be as higher as desired.

Simulation and Experimental Results

A Moving Average Filter is simulated in PSIM and experimentally tested in the float-point digital signal processor TMS320F28335. Two different signals are applied separately as input. It will be presented results for N=27 and N=54. Additionally, a step is made in the input signal and the filter dynamic behavior is evaluated. The digital results are obtained experimentally by means of a DAC (Digital-Analog Converter).

1) Sinusoidal signal as input

A sinusoidal signal is applied to the input of the filter. Its fundamental frequency is f_o=45Hz. The sampled frequency chosen is 20 times the fundamental frequency. It means,

$$f_s = 20 f_o \tag{4}$$

The Fig. 3 presents the analog signal and the digital sampled signal used as input of the moving average filter. Actually, this is the AC part of the signal. Such part is summed up to a 1.5V DC constant value, as will be presented later. The cursors indicate the 900Hz sampling frequency.

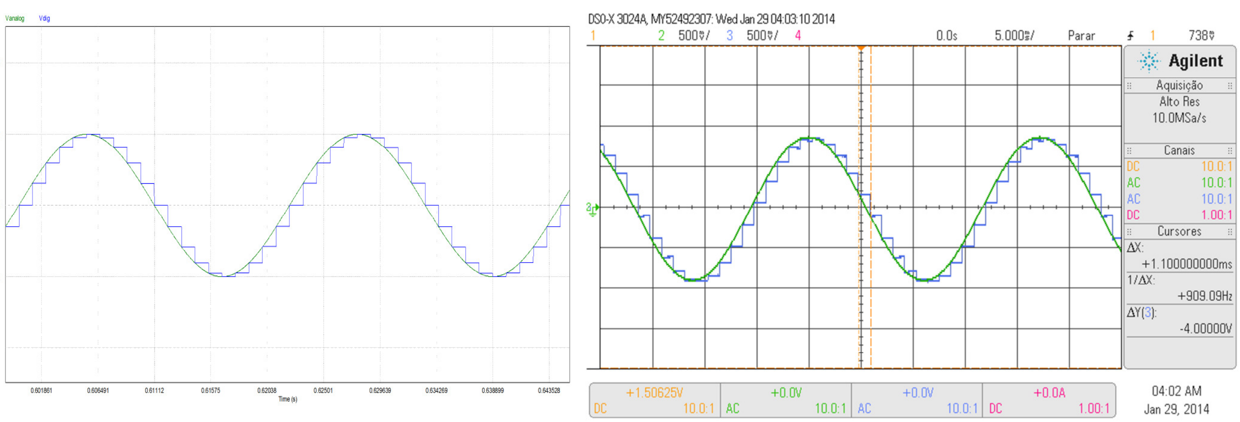

Fig. 3: The analog signal (green) and the digital sampled signal used as input.

The Fig. 4 presents again the above signal, but now with the DC value summed up and the output signal of the moving average filter for N=27 and N=54. Notice that the output signal for N=54 presents lower ripple than the output signal for N=27.

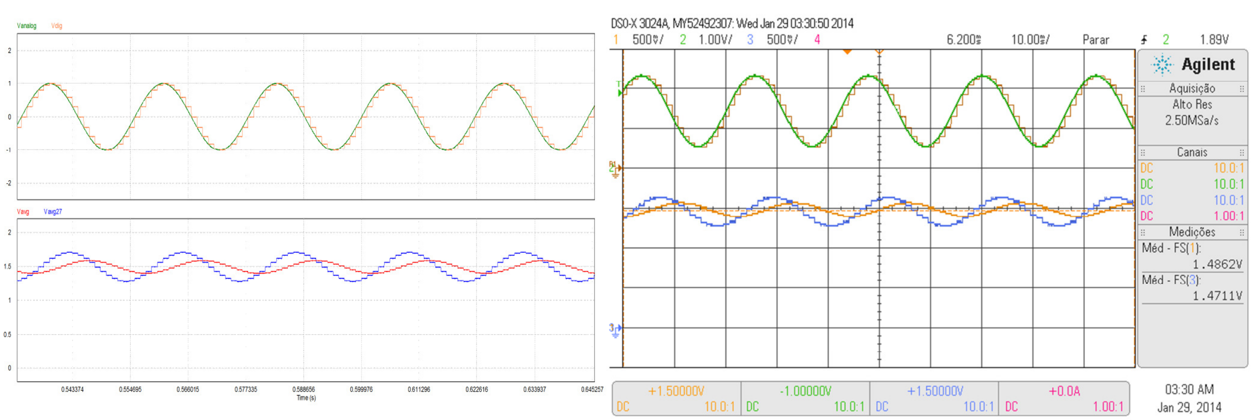

Fig. 4: The analog signal (green), the input signal (orange), the output signal for N=27 (blue) and N=54 (dark orange).

The Fig. 5 presents the output signal for N=27 and N=54 during a reference step. The step was applied to the DC value of the signal from 1.5V to 1.75V. Neither oscillatory nor unpredictable behavior has occurred.

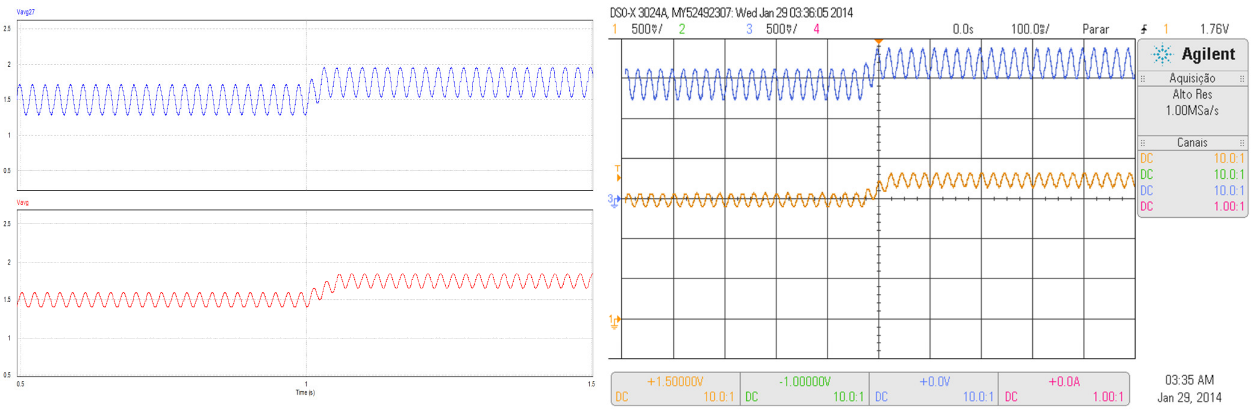

Fig. 5: Output signal for N=27 (blue) and N=54 during a reference step.

The Fig. 6 presents the output signal for N=54 and the reference step for comparisons.

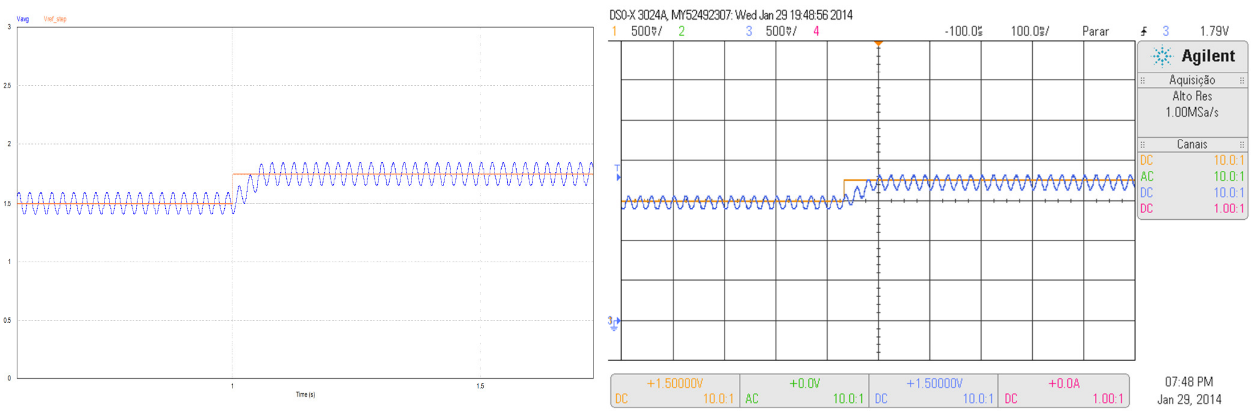

Fig. 6: Output signal (blue) and the reference step.

The Fig. 7 presents the same results, but now in detail.

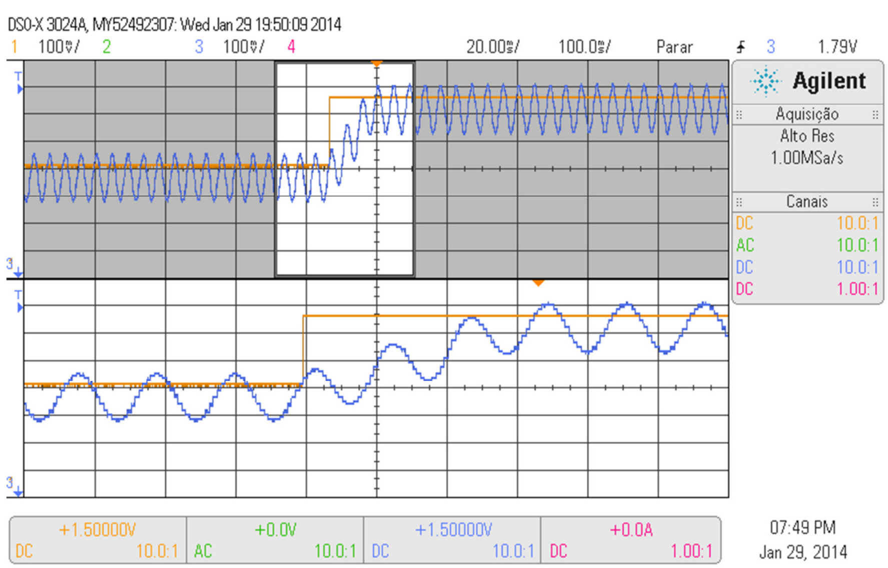

Fig. 7: Output signal (blue) and reference step in detail.

2) Distorted signal as input

The Fig. 8 presents the analog signal and the digital sampled signal used as input. The input signal is a sinusoidal summed up to the 25%, related to the fundamental, of 3rd harmonic component.

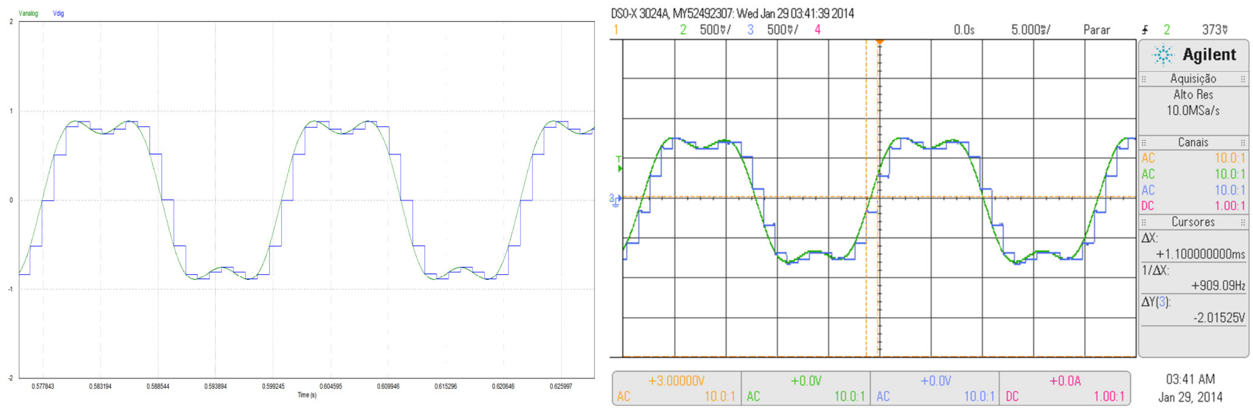

Fig. 8: Analog signal (green) and the digital sampled signal used as input.

The Fig. 9 presents the input and output signal during a reference step for N=54.

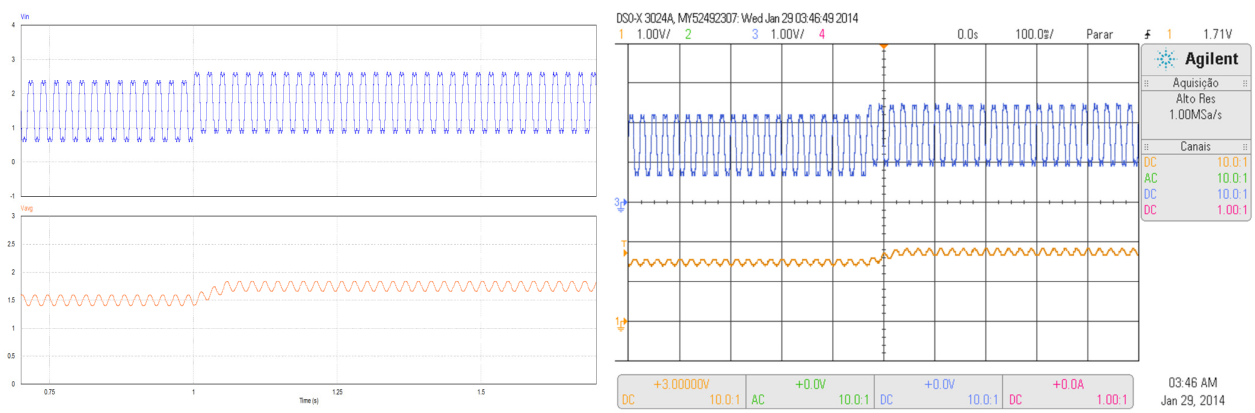

Fig. 9: Input (blue) and Output signal for N=54 (orange).

The Fig. 10 presents the dynamic behavior of the output signal during the start-up. The reference DC value was set to 2.25V. The steady-state condition is achieved without an unpredictable behavior. The 1.7 constant value before the start-up is presented due to the initial condition of the used DAC.

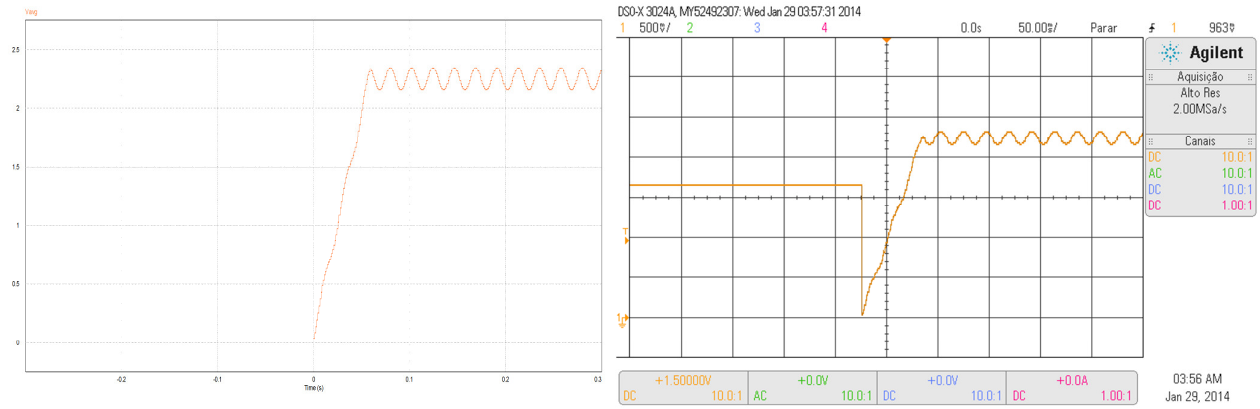

Fig. 10: Dynamic behavior during the start-up.

The Fig. 11 presents a part of the simulated circuit.

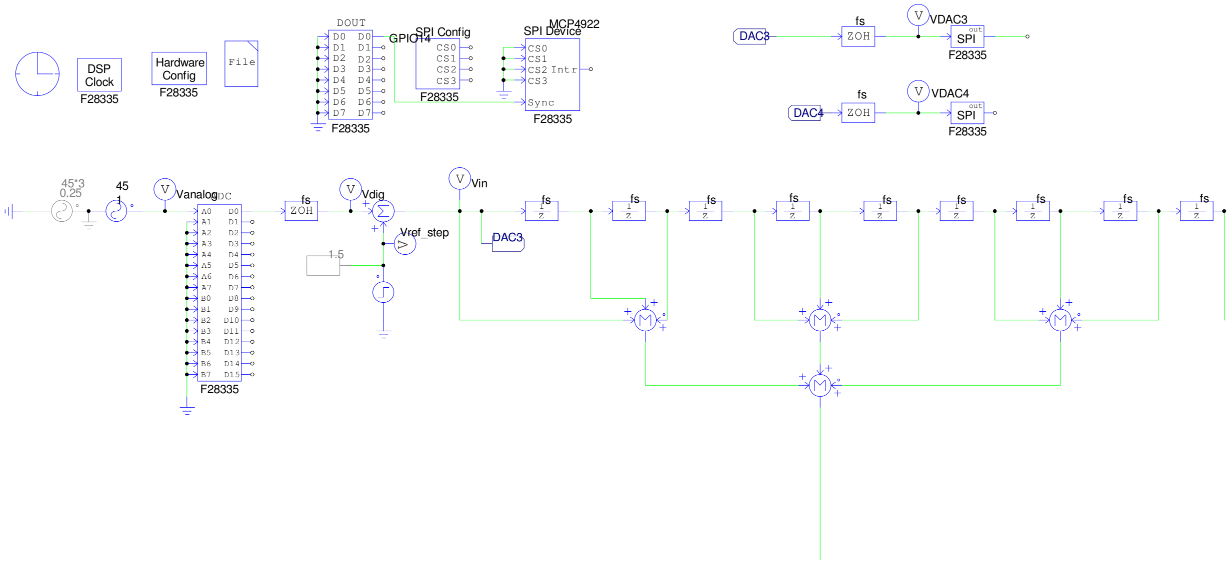

Fig. 11: A part of the simulated circuit

The complete simulation file with Automatic Code Generation used in this project is available for free on https://sites.google.com/site/busarellosmartgrid/

Reference:

[1] Richard G. Lyons. “Understanding Digital Signal Processing” Third Edition, Prentice Hall, 2011.